Application No.: 09/653,527 Docket No.: M4065.0814/P814 Amendment dated August 10, 2005

Reply to Office action dated June 2, 2005

REMARKS

Claims 1, 2, 6, 14, 15, 27 and 28 have been amended. No new matter has been

added.

Applicants graciously acknowledges the allowance of claims 7, 11-13, and 22-

26.

Claim 27 is objected to because the limitation "a gate of said first select

transistor" lacks sufficient antecedent basis. Claim 27 has been amended to depend from

claim 26, which contains sufficient antecedent basis. Accordingly, Applicants respectfully

request withdrawal of this objection.

Claim 28 stands rejected under 35 U.S.C. § 112, first paragraph, as failing to

comply with the written description requirement. Claim 28 previously stated that the gate

of the select transistor of the second pixel is connected to a third reset/select line. Claim

28 has been amended to recite that "a gate of said second reset transistor is connected to a

third reset/select line." This amendment is supported at least by FIG. 2 and the

corresponding description in the specification. Accordingly, withdrawal of this rejection is

respectfully requested.

Claims 1-3, 5, 6, 14, 15, and 27 stand rejected under 35 U.S.C. § 102(e) as

being anticipated by Chen, U.S. Patent No. 5,869,857. This rejection is respectfully

traversed.

As amended, independent claim 1 recites an image sensor comprising, inter alia,

"a plurality of pixels, each pixel having a photoreceptor therein, a follower transistor

connected to said photoreceptor, a select transistor connected to said follower transistor,

and a reset transistor which controls applying a reset level." Claim 1 further recites "a first

bias line providing power to at least a first of said transistors for a first pixel, and a second

bias line providing power to at least a second of said transistors of said first pixel different

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than said first transistor of said first pixel, such that said first and said second transistors are separately powered by separate bias lines, wherein said first bias line further provides power a said second transistor of a second pixel, and said second bias line further provides power to a said first transistor of a third pixel, and wherein a gate of said reset transistor of the first pixel is connected to a first reset/select line, and a gate of said select transistor of a different pixel is connected to said first reset/select line."

Amended independent claim 14 recites an active pixel sensor comprising "an array of pixels, each pixel comprising a photoreceptor, and at least first and second transistors associated with said photoreceptor in said each pixel, each first transistor of each pixel providing a same pixel function and each second transistor of each pixel providing a same pixel function, said first transistor of a first pixel connected to receive power from a first power supply source over a first line, and said second transistor of said first pixel connected to receive power from a second power supply source over a second line separate from said first power supply line, wherein said first transistor of said first pixel and said second transistor of a second pixel are connected to said first line."

Chen does not disclose all limitations of either of claims 1 and 14. Chen relates to a CMOS charge-integration mode photodetector. Chen at Abstract. Chen discloses that each photodecting element in an array have a photodiode and transistors M1, M2 and M3. In figures 10A, 11A, and 13A, Chen discloses a source/drain region of all transistors M3 are connected to Vbias, while a source/drain region of all transistors M1 are connected to VDD. Accordingly, Chen fails to disclose at least "said first bias line further provides power a said second transistor of a second pixel, and said second bias line further provides power to a said first transistor of a third pixel," as recited by claim 1; and "said first transistor of a first pixel connected to receive power from a first power supply source over a second power supply source over a second power supply source over a second line separate from said first power supply line, wherein said first transistor of said first pixel and said second transistor of a second pixel are

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connected to said first line," as recited by claim 14. For at least these reasons, withdrawal of this rejection is respectfully traversed.

Claims 8 and 9 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Chen in view of Merrill, U.S. Patent No. 5,614,744 (Merrill). This rejection is respectfully traversed.

As discussed above, Chen fails to disclose, teach or suggest all limitations of independent claim 1, from which claims 8 and 9 depend. Merrill is cited for disclosing a photogate, floating diffusion portion and transfer gate. Merrill, however, fails to supplement the deficiencies of Chen. Specifically, like Chen, Merrill fails to teach of suggest at least "said first bias line further provides power a said second transistor of a second pixel, and said second bias line further provides power to a said first transistor of a third pixel," as recited by claim 1. Therefore, even when considered in combination, these references do not teach or suggest all limitations of independent claim 1, or claims 8 and 9 depending therefrom. For at least these reasons, withdrawal of this rejection is respectfully requested.

Claim 16 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Chen in view of Okamoto, U.S. Patent No. 6,580,063 (Okamoto). This rejection is respectfully traversed.

As discussed above, Chen fails to disclose, teach or suggest all limitations of independent claim 14, from which claim 16 depends. Okamoto is cited for disclosing a steady state current generator. Like Chen, however, Okamoto fails to teach or suggest "said first transistor of a first pixel connected to receive power from a first power supply source over a first line, and said second transistor of said first pixel connected to receive power from a second power supply source over a second line separate from said first power supply line, wherein said first transistor of said first pixel and said second transistor of a second pixel are connected to said first line," as recited by claim 14. Accordingly, even

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when considered in combination, Chen and Okamoto fail to teach or suggest all limitations of independent claim 14 or dependent claim 16. For at least these reasons, withdrawal of this rejection is respectfully requested.

In view of the above amendment, applicants believe the pending application is in condition for allowance.

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Respectfully submitted,

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